Assam Textile Institute

Empowering Textile Education

Class 6

COURSE TITLE = TEXTRONICS

COURSE CODE= TT-603

by,

PANKAJ JYOTI DAS

(M.TECH),(ECE)

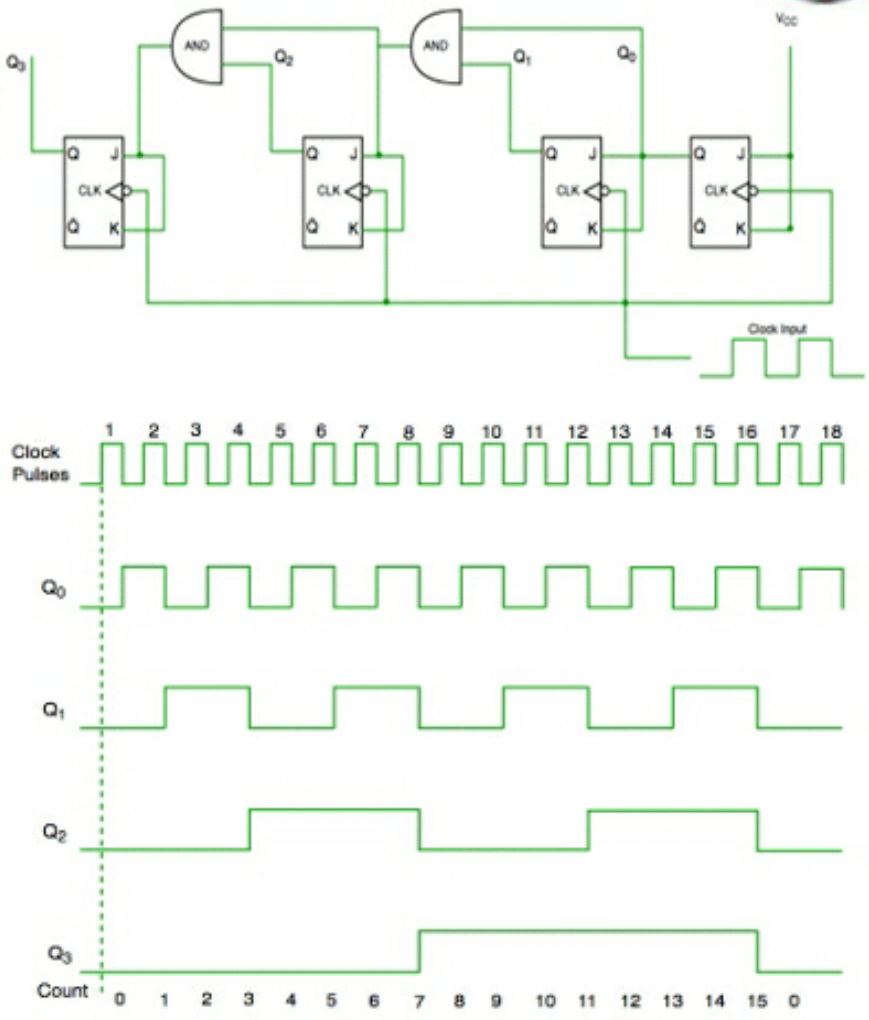
: Counters in Digital Logic :

2. **Synchronous Counter**

Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel.

The one *advantage* of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.

It is shown in timing diagram that that Q0 bit gives response to each falling edge of clock while Q1 is dependent on Q0, Q2 is dependent on Q1 and Q0 , Q3 is dependent on Q2,Q1 and Q0.

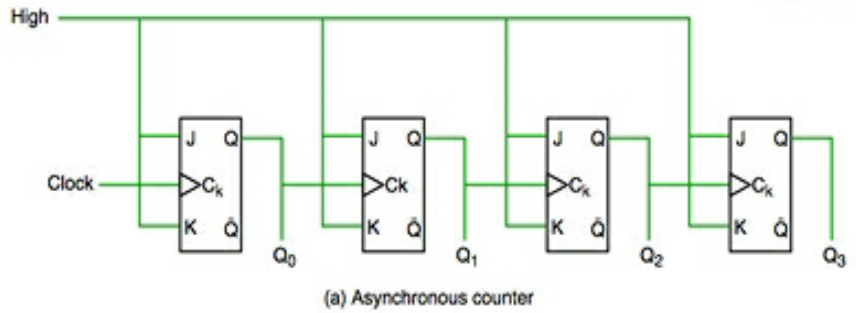


: Counters in Digital Logic :

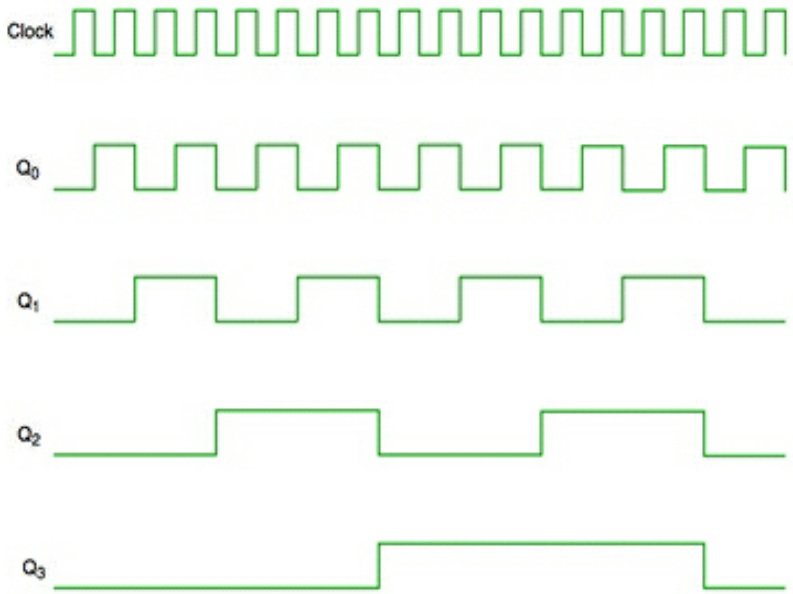
1. Asynchronous Counter

In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following counters is driven by output of previous flip flops.

It is shown in timing diagram that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered(because Q0 is like clock pulse for second flip flop) and so on. In this way ripples are generated through Q0,Q1,Q2,Q3 hence it is also called **RIPPLE counter.**



(a) Asynchronous counter



(b) Timing Diagram

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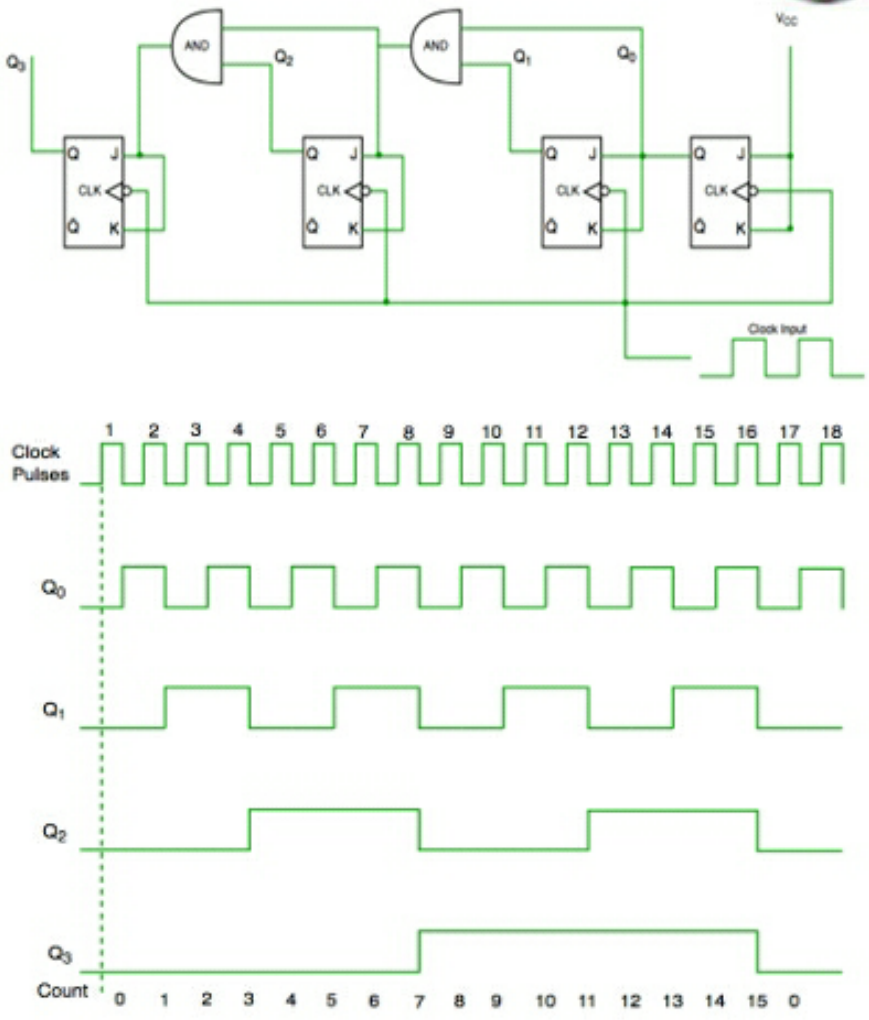
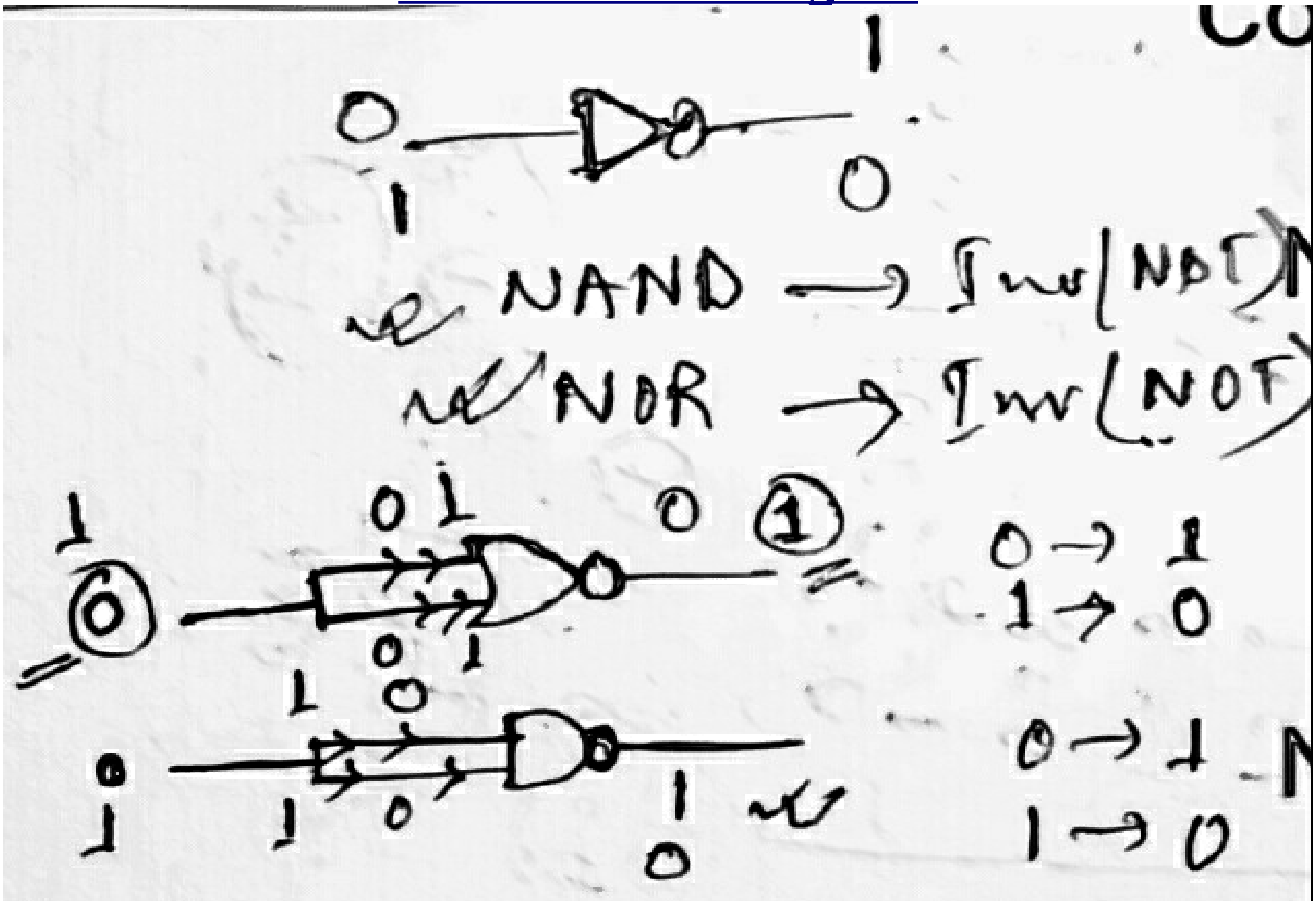
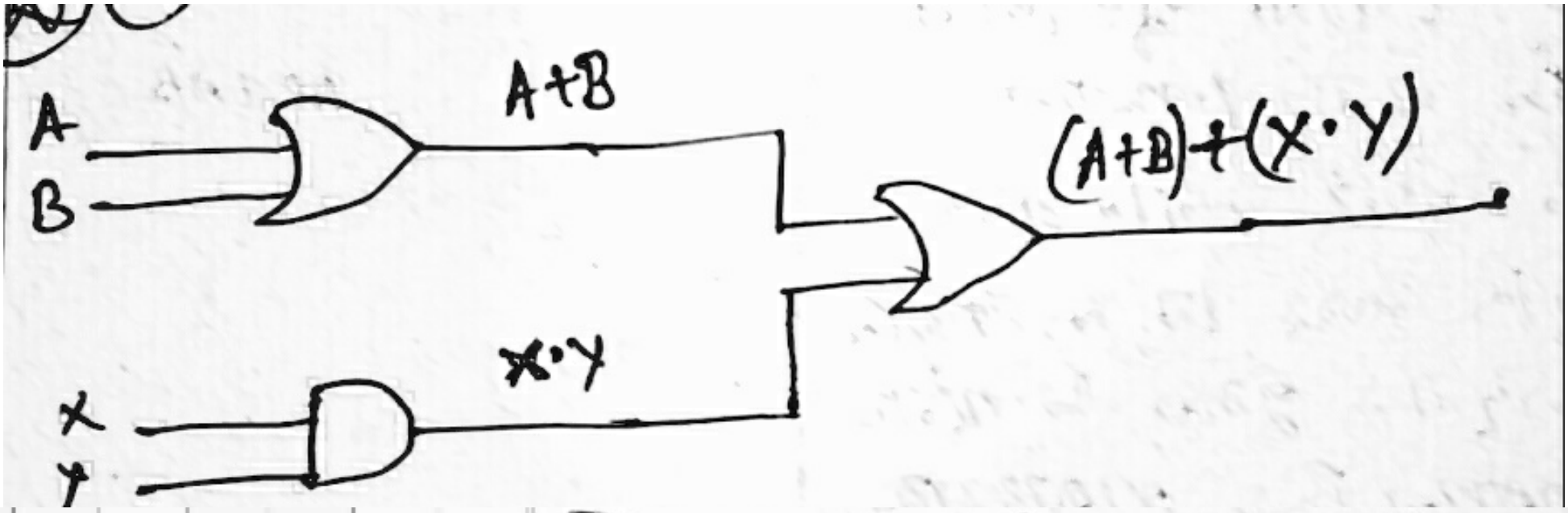
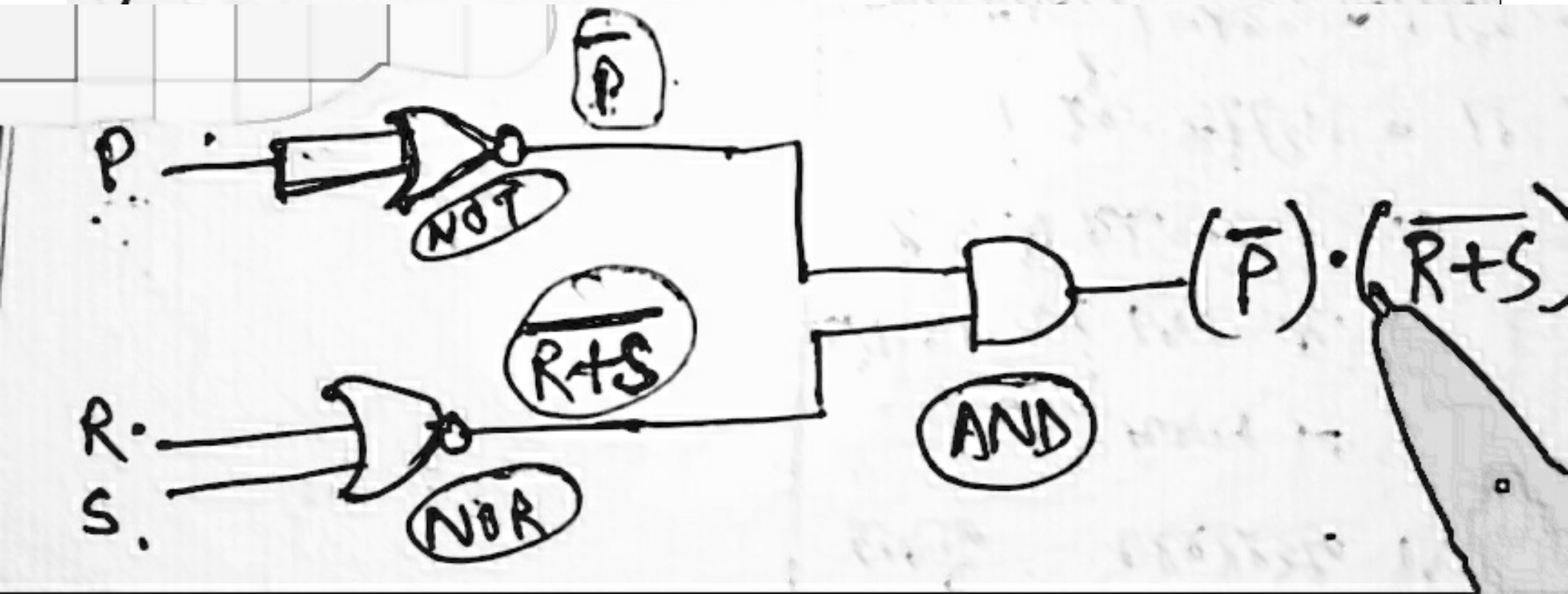


Construction of NOT gate by using NOR and NAND gate



LOGIC GATES PROBLEM





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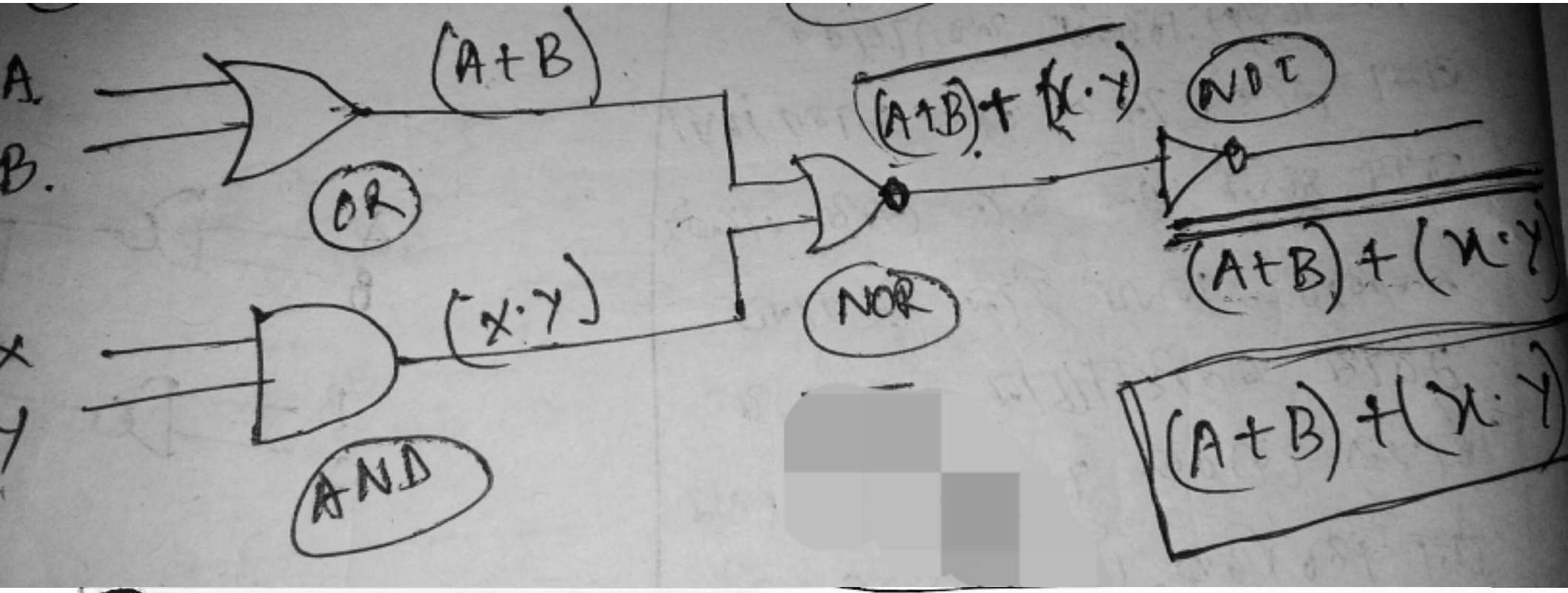

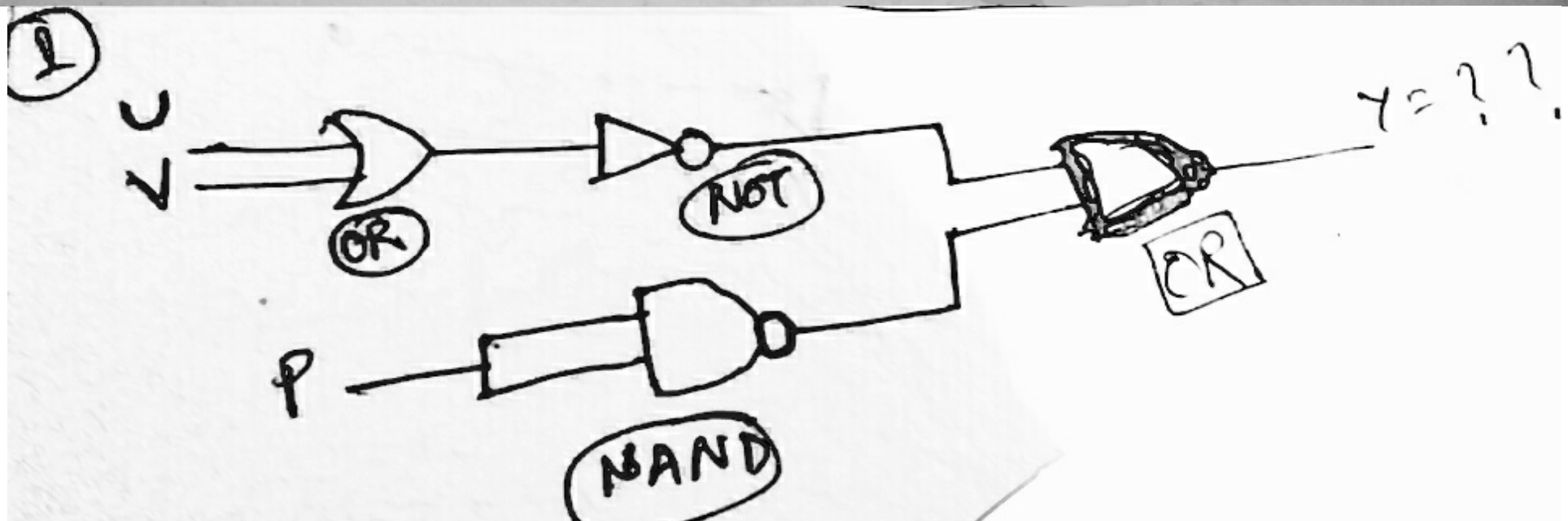

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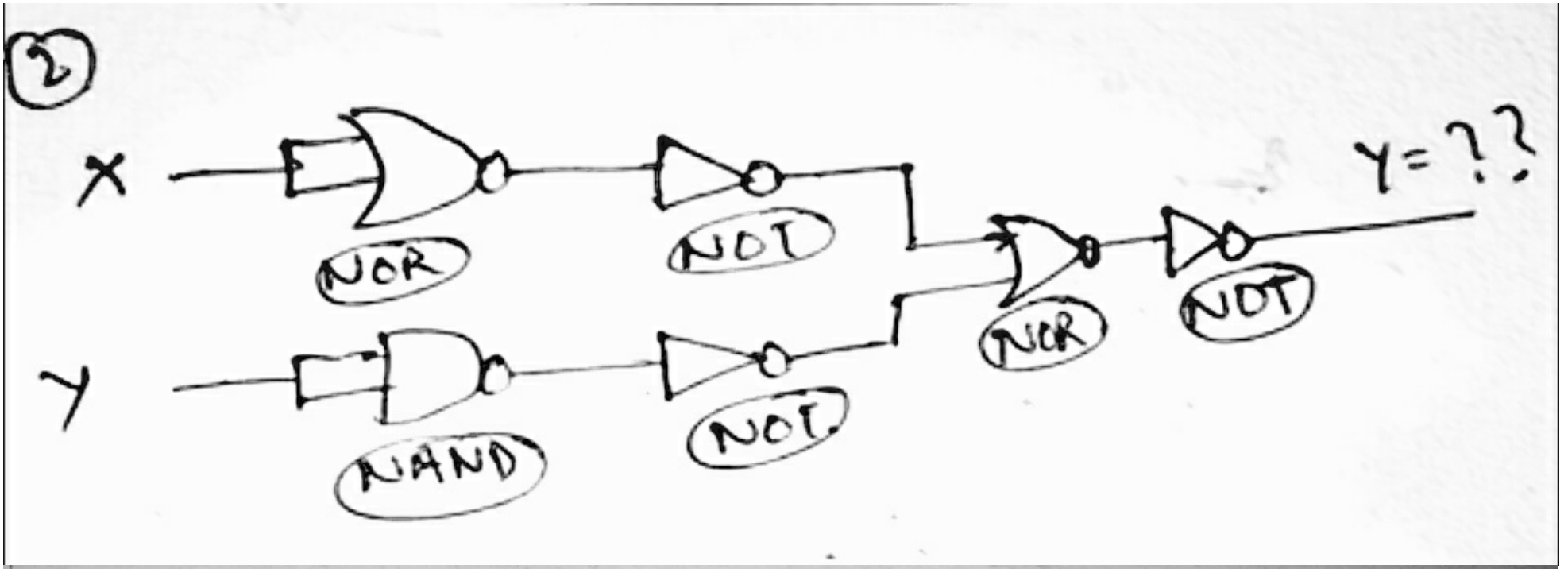

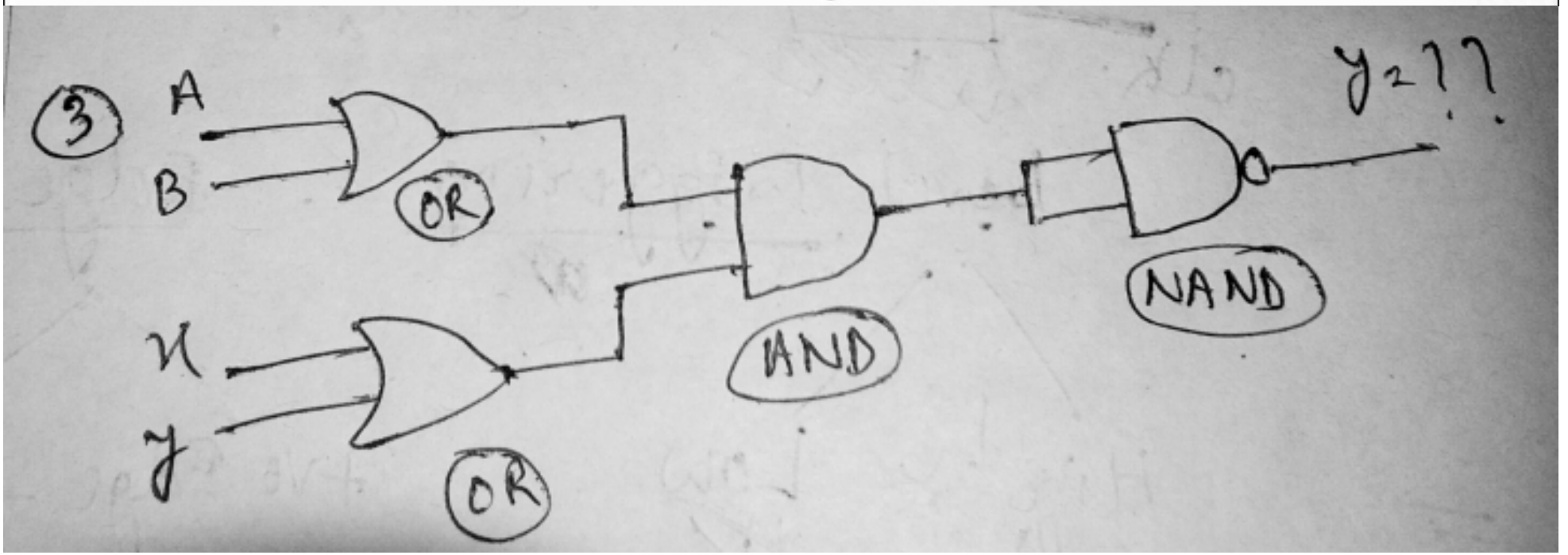

LOGIC GATES PROBLEM